A Compact Neural Network for High Accuracy Bioimpedance-Based Hand Gesture Recognition

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***Abstract*— This paper presents a compact customised neural network with 44 parameters for hand gesture recognition based on electrical impedance tomography (EIT) using a flexible 8-electrode band. The classification accuracy is improved by assigning higher weights to the impedances captured closer to the current injection position. The non-fully connected layer working as a spatial filter reduces the complexity of the network structure. Validated on a discrete EIT system, the proposed network structure can distinguish eight gestures with an accuracy of 99.49%. Towards a low-power wearable design, an analogue inference circuit based on the proposed network structure was also designed in 65 nm CMOS. The system features a low-power multi-output digital-to-analogue converter (DAC) to provide data for the analogue computation efficiently. This designed CMOS analogue inference has a recognition accuracy of 98.13%.**

Keywords—Analogue computation, electrical impedance tomography, hand gesture recognition, neural network.

I. Introduction

Electrical impedance tomography (EIT) has been extensively developed for hand gesture recognition, providing information on muscle contraction and bone movement [1]-[8]. This technique allows a human-machine interface (HMI) to control a robotic hand or prosthesis [1]. It also has potential for applications in virtual reality interaction, sign language recognition and intelligent robot control.

Unlike conventional EIT, which uses an inverse solver to produce images, EIT-based HMI employs recognition algorithms to link the data to, for example, hand gestures. Current recognition algorithms can be divided into two main categories. (i) image-based: convolution neural network (CNN) is employed to classify the EIT image reconstructed by finite element method [2], [5]; and (ii) non-image based: the impedance data is directly provided to machine learning algorithms, for example, support vector machine (SVM), k-nearest neighbours (KNN) and decision tree (DT) [1], [6]. These algorithms are designed to run on a standard personal computer (PC) and are generic in nature. Implementing them on a wearable edge computing device for extended periods of use poses a significant challenge regarding power and hardware resources.

In addition, using a high number of electrodes provides higher recognition accuracy but at the expense of hardware resources. Common electrode configurations worn on the forearm have a single 8-electrode band [1]-[3], a single 16-electrode band [4], [5] or two bands each with 8 electrodes [6]. Some studies also investigated electrodes attached directly to the back of the hand for better selectivity [7].

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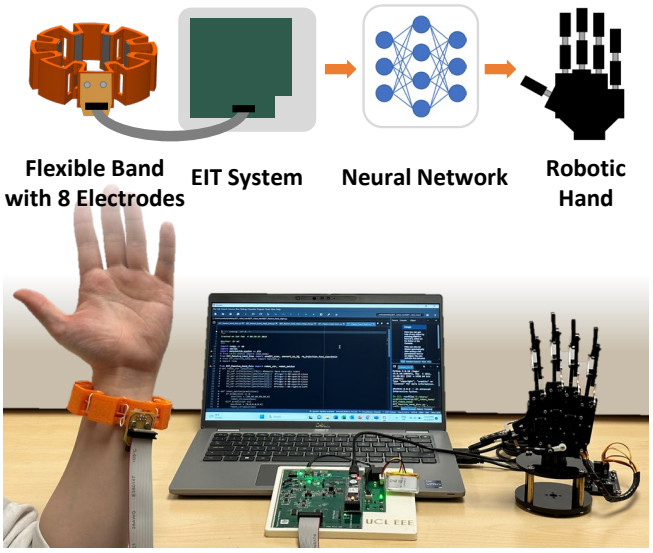

Fig. 1. Hand gesture recognition system based on bioimpedance measurement.

Analogue signal processing (ASP) applied successfully to machine learning systems can achieve much higher energy efficiency compared to their digital counterparts [9]. In order to do so, energy-efficient analogue computations exploit the characteristics of transistors operating in the subthreshold region [10]. Currently, mixed-signal systems are the dominant approach. For instance, in [9], a mixed-signal architecture was proposed where analogue computation was used for mathematical operations such as multiplication, square root, and Gaussian function. On the other hand, in [11], a dual-mode architecture was proposed in which digital and analogue modules in the machine learning system were switched depending on the scenario.

This paper presents the design of a compact, lightweight neural network optimised for EIT datasets applied to hand gesture recognition. The work consists of three main parts. (i) Design of an EIT-based HMI system with 8 electrodes for data capture, as shown in Fig. 1. The EIT data is captured using a high-performance system that can record 256 bioimpedance features every 10 ms [12]. (ii) Analysis of the captured bioimpedance features to design a lightweight neural network. The proposed network only requires 33 weights and 11 biases compared to other networks [2], [5] that have thousands of parameters. (iii) Based on the designed compact neural network, an inference engine was implemented in TSMC 65 nm CMOS technology using ASP to reduce power consumption and computational resources.

The rest of the paper is organised as follows. Section II describes the structure of the compact neural network and its

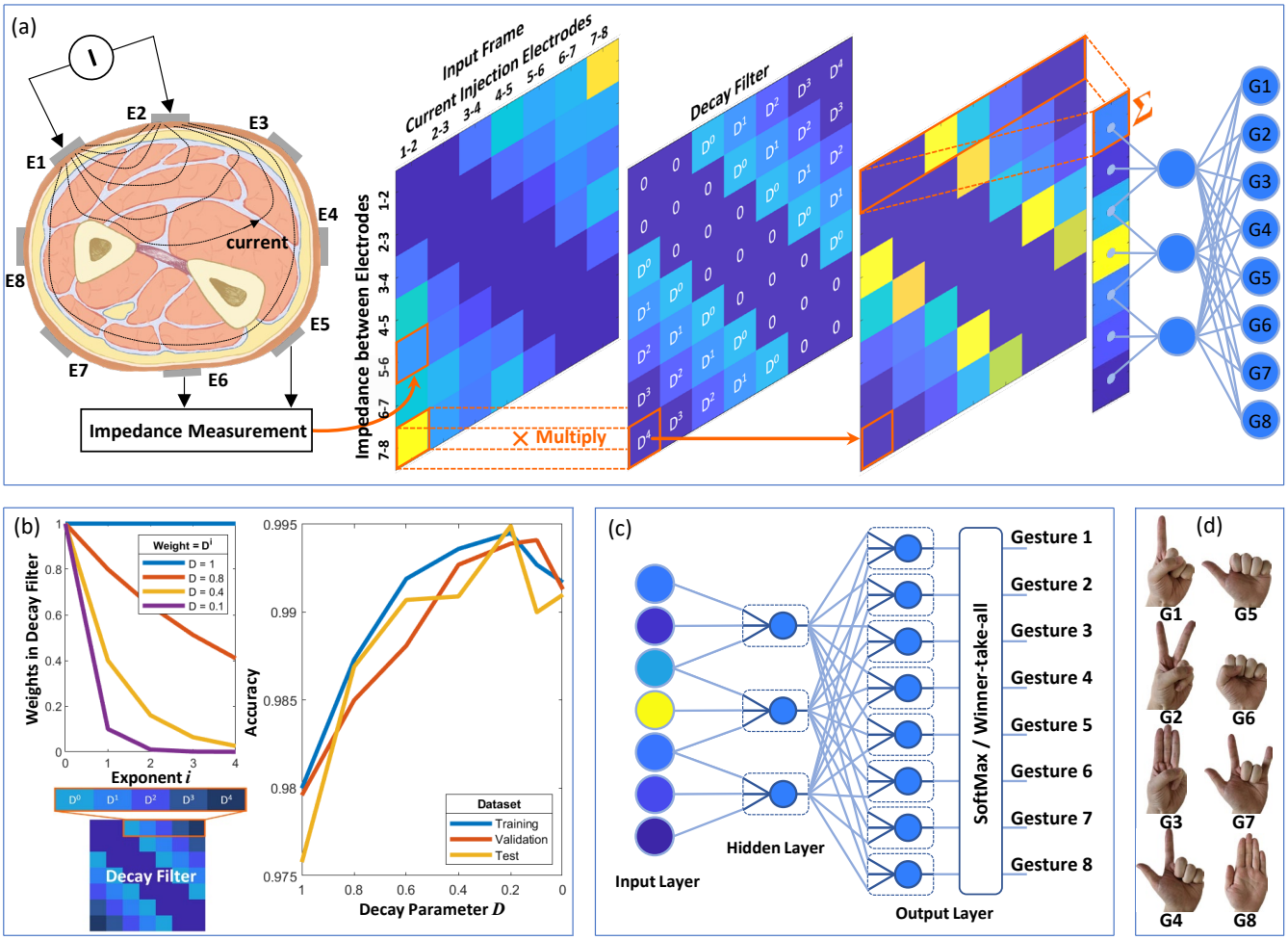

Fig. 2. The proposed compact neural network for hand gesture recognition. (a) Neural network architecture. (b) Effect of filter weight on accuracy. (c) Simplified network with identical nodes. (d) Eight hand gestures.

performance. Section III presents the analogue integrated circuit implementation of the neural network. Conclusions are drawn in Section IV.

II. Neural Network Structure

For general neural network applications, standard layers with numerous parameters of different types of neural networks are often used and trained with significant power and time resources. In contrast to this time and energy-consuming process, the approach proposed in this paper starts with reducing the number of parameters through processing the EIT data.

To achieve good resource efficiency, only 49 impedance features captured from 8 electrodes on a stretchable band were used in this work. In Fig. 2(a), one frame of impedance data is obtained from the EIT system. The seven elements in each column vector in the input frame are impedance values from all adjacent electrodes at each current injection position obtained using in-phase and quadrature-phase (I-Q) impedance demodulation. The impedance associated with electrodes used for current injection is set to zero in the input frame, because only voltages from the recording electrodes are used in EIT.

The closer the electrode is to the position where the current is injected, the higher the signal-to-noise ratio of the voltage recorded because of the higher current density. Leveraging this unique EIT pattern, a decay filter is proposed to provide a higher weight to the impedance derived from the position closer to the current injection position. After filtering the undesired impedance features, seven values are obtained by summing up each row as the input for the neural network. A non-fully connected layer, inspired by the bandpass spatial filtering of the retina [13], followed by a fully connected layer with eight outputs, is introduced to reduce the complexity of the connection between two layers and the redundancy of features. The structure from local impedance features to final prediction consists of 11 identical units, each with three inputs and one output, as shown in Fig. 2(c), which can better facilitate the design of the analogue inference.

To validate the proposed neural network structure, an EIT dataset was captured. It contains data from five subjects (4000 frames each), which was used to find the optimal weights in the decay filter. The dataset included eight gestures, as shown in Fig. 2(d), and a parameter D ranging from zero to one is defined as the base of a power. 70% of the dataset is used for training, 15% for test and the remaining 15% for validation. The recognition accuracy is plotted in Fig. 2(b) as parameter D varies. It can be seen that gesture recognition accuracy increases as parameter D decreases. When D is less than 0.4, the accuracy of the proposed neural network exceeds 99%.

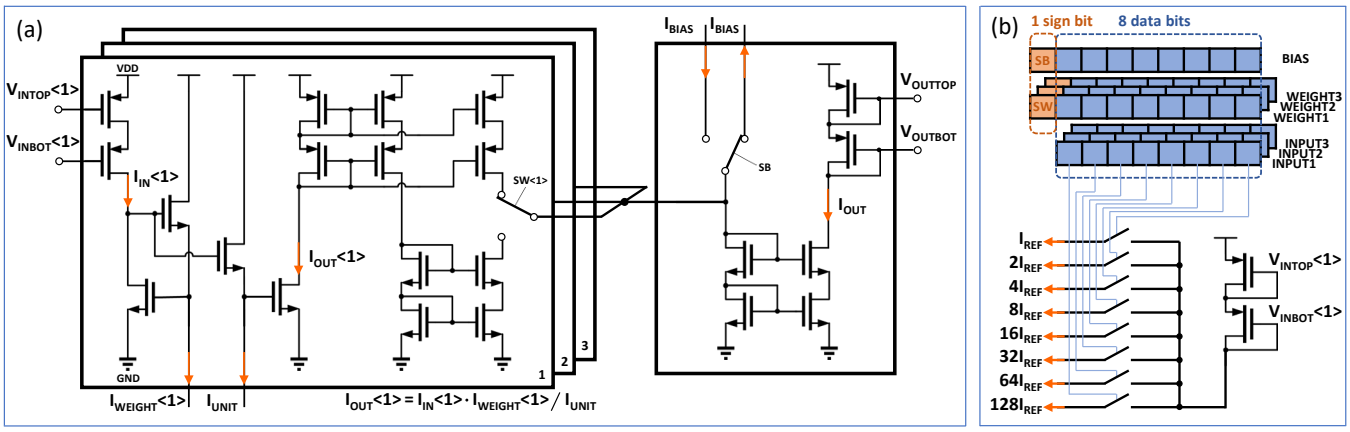

Fig. 3. Node structure. (a) Schematic of node. (b) Data saved in each node of hidden layer.

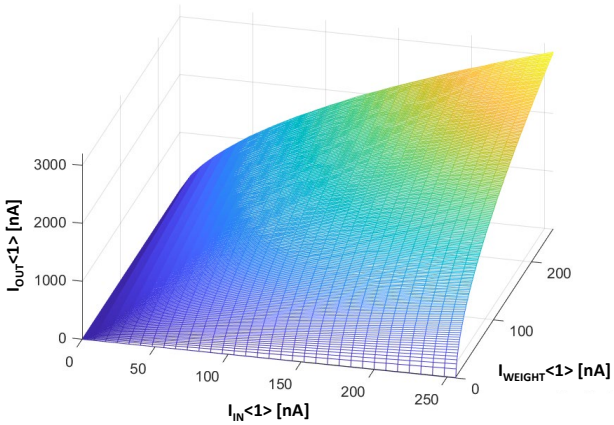

Fig. 4. Characteristics of the analogue current weighting.

III. CMOS Implementation of Neural Network

A. Nodes in Neural Network

The nodes with three inputs shown in Fig. 2(c) can be implemented in the CMOS for low power consumption. This design adopts current mode translinear circuits as analogue multipliers to calculate the input times weight. Owing to the fixed output current direction, the rectified linear unit (ReLu) activation function is naturally applied to the output. The inputs and parameters are saved in an SRAM array in 8-bit format with one sign bit, as shown in Fig. 3(b), and then they are converted to current signals by a current mode digital-to-analogue converter (DAC). For the hidden layer nodes, three inputs, three weights and one bias are required. For the output layer nodes, only three weights and one bias are needed. Inside the hidden layer nodes, the output current is converted into bias voltages of the cascode current mirror for front propagation, with minimal loss to the signal due to the capacitive load. The parameters are stored locally in the nodes for easy access during parallel computing.

As shown in Fig. 4, when the input and weight increase simultaneously, the output current gradually plateaus because the large current forces the transistors' gate-to-source voltage (VGS) close to the threshold voltage. The output characteristic no longer follows the well-known exponential law. Nevertheless, the non-linearity of the output current, treated as an activation function, is consistent with the dynamic model of real neurons and has minimal influence on the accuracy of prediction.

B. Current Mode Digital-to-Analogue Converter

To provide 44 parameter currents and 7 input currents simultaneously for parallel computing, a compact multi-bias DAC is proposed and shown in Fig. 5(a). The currents of inputs or parameters are generated by summing the selected currents among the eight reference currents. The reference currents are generated by eight pairs of identical transistors biased by different voltages. When transistors are in the subthreshold region and $V_{DS} > 4U_t$, where U_t is the thermal voltage, I_{BIT}<0> can be defined as

$$I_{BIT}\text{<0>} = I_0 \exp(\frac{V_{BIASBOT}\text{<0>}}{nU_t}) \quad (1)$$

where I_0 is W/L times characteristic current I_{D0}, and $n = 1 + C_D/C_{ox}$ is the slope factor [10]. Thus, the ith reference current can be ideally expressed as

$$I_{BIT}\text{<}i\text{>} = 2^i \times I_{BIT}\text{<0>} = I_0 \exp(\frac{i \ln 2 \times nU_t + V_{BIASBOT}\text{<0>}}{nU_t}). \quad (2)$$

Hence, the bias voltages can be given as

$$V_{BIASBOT}\text{<}i\text{>} = i \ln 2 \times nU_t + V_{BIASBOT}\text{<0>}. \quad (3)$$

It is demonstrated that the eight pairs of bias voltages can be obtained by equally dividing the voltage between $V_{BIASBOT}$<7> and $V_{BIASBOT}$<0>. The voltage difference between adjacent bias voltages is

$$\frac{V_{BIASBOT}\text{<7>} - V_{BIASBOT}\text{<0>}}{7} = \ln 2 \times nU_t. \quad (4)$$

When $V_{BIASBOT}$<0> is set to 240 mV, I_{BIT}<0> is approximately equal to 0.7767 nA. $V_{BIASBOT}$<7> is implemented by 128 times I_{BIT}<0> generated by the current mirrors. The large resistance of these series resistors is required to reduce the current between two reference voltages. The transistors operate as resistors accordingly while saving area. The transistors' gate and drain are connected, and the body is connected to the source. Cascode current mirrors with two resistor voltage dividers are adopted to improve the uniformity of voltage division, as shown in Fig. 5(b). The bias voltages generated from two voltage dividers are shared with all current sources in the hidden layer and the output layer. This power-efficient and area-friendly digital-to-current method combines the merits of stable digital memory and low-power analogue computation. However, the reference currents cannot strictly follow (2) due to nonidealities. The INL and DNL of the DAC are shown in Fig. 5(c). However, these nonidealities will not significantly impact the accuracy of the

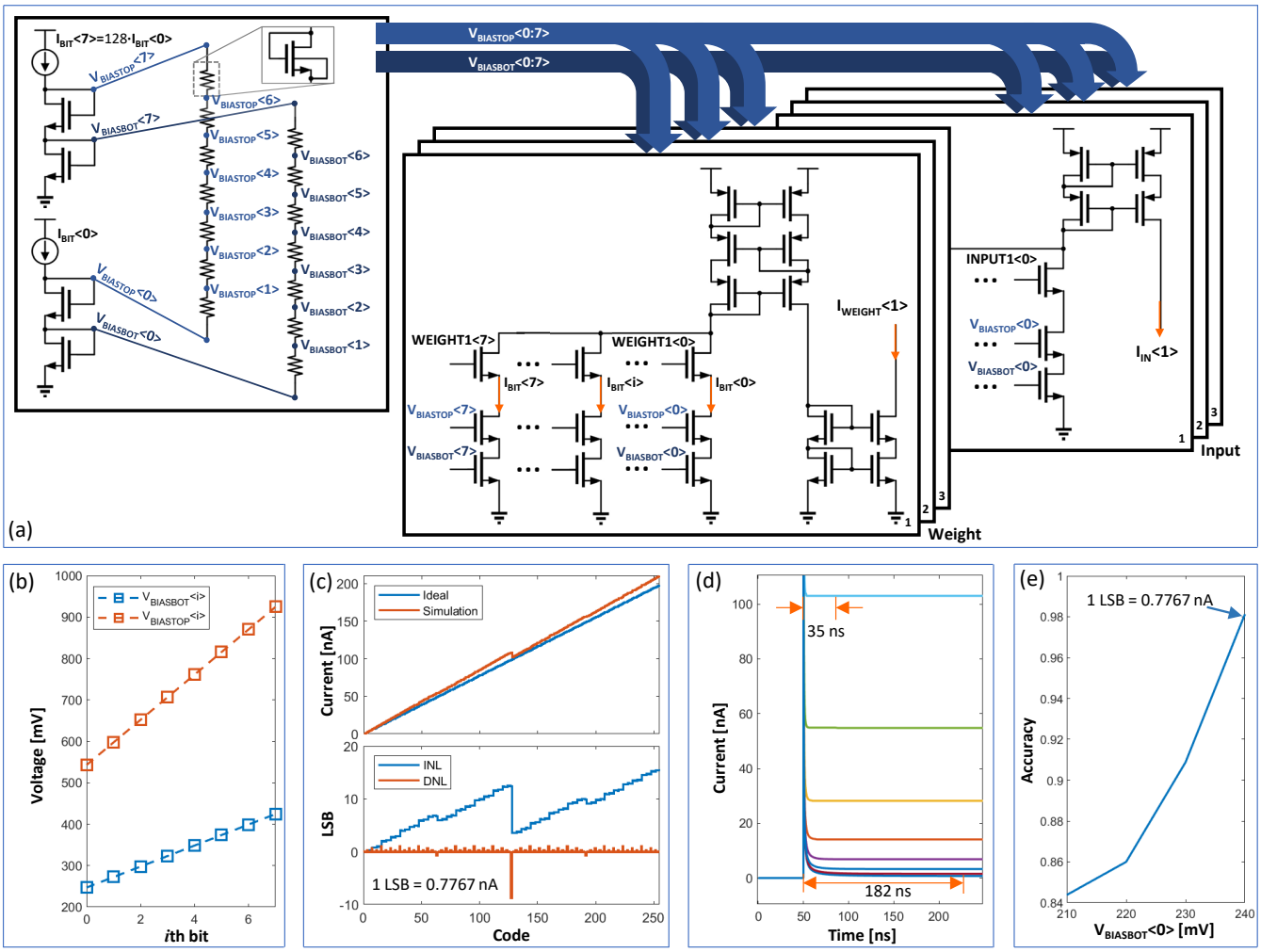

Fig. 5. A compact digital-to-current converter (DAC). (a) Structure of the DAC. (b) Bias voltages for cascode current mirrors. (c) INL and DNL. (d) Setup time. (e) Accuracy variation with bias voltage.

TABLE I. COMPARISON WITH OTHER WORK

Parameter	[1]	[2]	[3]	[5]	This work
Electrodes	8	16	8	16	8
Gestures	5+5+3[1]	10+Rest position	9	7	8
Algorithm[2]	ANN	CNN	Quadratic Discriminant	CNN	Customized NN
Network Parameters	>4100	>2300000	-	>1000000	44
Accuracy	95.8%	95.94%	98.5%	93%	99.49%

[1] Hand gesture multi-group used.
[2] List the algorithm with the highest accuracy.

analogue network. In terms of response time, the longest setup time is around 182 ns, which is sufficient for the frame rate of the EIT system, as shown in Fig. 5(d). Lastly, the reference currents can be further scaled down to reduce power consumption but at the expense of accuracy, as shown in Fig. 5(e).

C. Analogue Neural Network

Using the node design in Fig.3 and the DAC in Fig.5, a compact analogue neural network was implemented following the structure shown in Fig. 2(c). A winner-take-all circuit is used as the output layer, and its current outputs can be used to present the gesture outcome. The accuracy of the analogue inference is 98.13%, with a typical power consumption of 20 µW. A comparison against the state of the art is presented in Table I. This work achieves comparable accuracy using a significantly smaller number of neural network parameters.

IV. CONCLUSION

This paper has proposed an efficient method to scale down the size of the neural network for bioimpedance-based hand gesture recognition. Using the data captured from a discrete EIT system, the proposed neural network is first validated on MATLAB. It can classify eight hand gestures with an accuracy of 99.49%. In addition, an analogue inference has been designed in CMOS technology. This inference features a low-power analogue node and multi-output DAC. The accuracy of this implementation is up to 98.13%, with a power consumption of 20 µW. Future work will focus on developing an on-chip training method to compensate for process, supply voltage and temperature (PVT) variations for the analogue neural network.

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